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LETTER

A Low Voltage High Speed Self-Timed CMOS Logic for the Multi-Gigabit Synchronous DRAM Application

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SUMMARY A low voltage dual V_T self-timed CMOS logic in which the subthreshold leakage current path is blocked by a large high-V_T MOS is proposed. An active signal at each node of the self-timed circuit resets its own voltage to its standby state after 4 inverter delays. This pulsed nature speeds up the signal propagation and enables the synchronous DRAM to adopt a fast pipelining scheme.

key words: *low voltage, self-timed CMOS logic, synchronous DRAM*

1. Introduction

The supply voltage of 1.5 V or below is expected to be used in multi-giga bit DRAM's not only to reduce the power consumption but also to enhance the reliability of the scaled devices [1]. To maintain the high speed operation of the DRAM even with this low supply voltage, the threshold voltage of the MOS has to be scaled down because the current of the MOS depends on the difference between the supply voltage V_{DD} and V_T. However, as V_T decreases, a large amount of standby current results from the exponential increase of the subthreshold leakage. In 16 Gbit DRAM whose total channel width of MOS transistors amounts to 16 m, the dc standby current generated by the subthreshold leakage current is expected to exceed the ac operating current, because the subthreshold current depends linearly on the channel width of the MOS transistor [2].

The dual V_T logic was proposed to resolve the subthreshold current problem [3]. It is useful in DRAM design where the standby state of each node was known explicitly during design period. A large high-V_T MOS is used to block the subthreshold current flow from its output node to power or to ground line in standby state. And a small low-V_T MOS of opposite polarity is used to hold the standby voltage at its output node. This connection scheme can reduce the subthreshold current and the standby to active transition time. On the other hand, the active to standby transition is delayed as the ratio γ of the width of high-V_T MOS to that of low-V_T MOS increases. By taking both transitions into account, γ for the smallest propagation delay can be optimized to be 0.26 [3], which results in far lower speed than that obtained from the single low-V_T logic. In this letter, a new dual V_T self-timed logic is proposed, which combines only the strong points of the single low-V_T logic and the dual V_T logic; i.e., high speed and low subthreshold current.

2. Circuit Description

In the dual V_T logic, an input transition turns off a small low-V_T MOS that had been holding its standby voltage as well as turns on a large high-V_T MOS of opposite polarity to switch its output to active state. An inverter must charge up two gate capacitances of the next stage. In the circuit proposed in this letter, however, each logic stage drives only one high-V_T transistor at the following stage. Figure 1 shows the detailed circuit topology of the proposed self-timed dual V_T logic. In the first place, the external input signal, usually active low in DRAM operation, is transformed into a negative pulse with finite width by a negative edge detector circuit. The pulse width is chosen to be 5 inverter delays and the width is maintained constant along the propagation path by the feedback resetting circuit which has the same delay as that of the edge detector. Since the edge detector does not affect the speed of the circuit, high-V_T P- and N-MOS's are used to reduce the subthreshold current. For the present, an assumption is made that all nodes are initially at their standby voltage levels. These standby states alternate between "H" for all odd numbered nodes and "L" for all even numbered nodes as shown in Fig. 1. A negative transition at the input node of the first stage drives P_1 and pulls up its output to its active state, "H." This transition turns on N_2 of the second stage and pulls down its output to its active state, "L." These active transitions propagate through the circuit very quickly because input signals charge the capacitance of only one MOS gate in contrast to the conventional CMOS logic which needs to drive two gate capacitances. The width of the high-V_T MOS can be increased without increase of transition time from active to standby state because a separate signal path resets its output automatically. In addition, even the supply voltage can be reduced because each stage is

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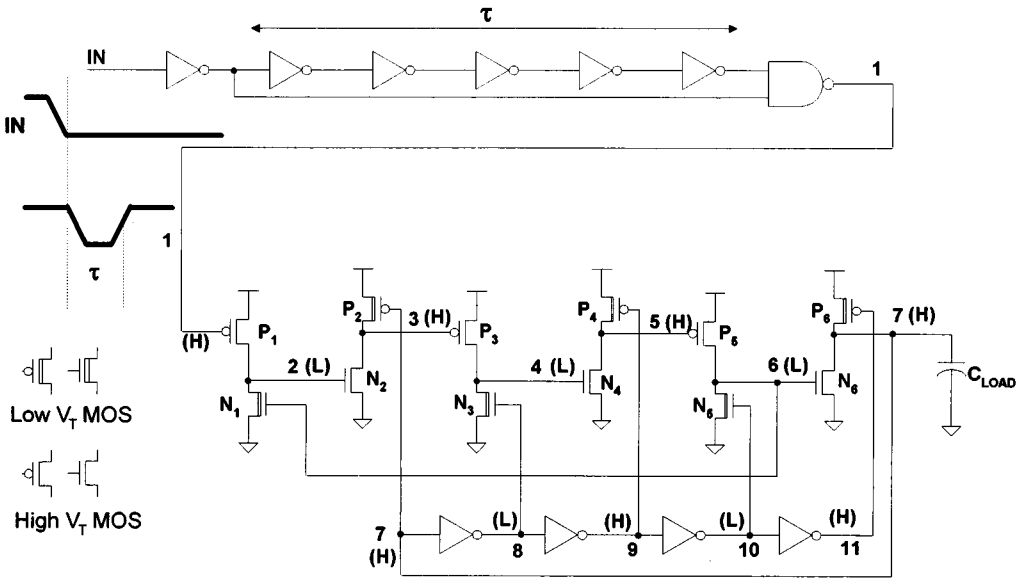

Fig. 1 A schematic circuit diagram of the dual V_T self-timed CMOS logic. It is composed of an edge detector circuit, a 5 inverters chain, a feedback path and a load capacitor C_{LOAD} (=3389 μm MOS width).

composed of only one MOS instead of serial connection of P-MOS and N-MOS as is the case for the conventional CMOS logic.

The active to standby resetting transition is made by a low-V_T MOS of opposite polarity. The resetting transistors are enabled by standby to active transition voltages at output nodes of 4 stages ahead. For example, the active transition at node 6 turns on the resetting low-V_T N-MOS N_1 as well as turns on high-V_T N-MOS N_6 of the next stage. Therefore, each node resets to its standby state automatically after 4 inverter delays. Since the inverter fan-out is larger than one, usually 3, the width ratio of the n-th resetting transistor to $(n-4)$-th active transistor, for example N_1/N_6, is negligibly small. In addition, the same current drivability can be obtained from the low-V_T MOS transistors with far smaller width than that of the active high-V_T transistors. That is, the width of the low V_T MOS which has the same current drivability as the high V_T MOS is given as $W_L = W_H(V_{DD}-V_{TH})^2/(V_{DD}-V_{TL})^2$, where W_L, W_H, V_{TH} and V_{TL} are the width of low V_T MOS, the width of high V_T MOS, the threshold voltage of the high V_T and the threshold voltage of the low V_T MOS, respectively. This allows a big ratio between the active high-V_T MOS and the resetting low-V_T MOS, and each transition, active to standby or standby to active, can be optimized separately to obtain very fast symmetrical transitions.

It is widely accepted that synchronous memories will be major in giga bit DRAM era due to its speed compatibility with the microprocessor [4]. The synchronous memory must generate a fast stream of data in response to changes of column addresses, such as burst read operation in a synchronous DRAM. In this fast access mode, not only the fast active transition but also the fast resetting transition are required. The proposed circuit meets these requirements inherently. In addition, due to its finite pulse width, even plural pulses propagate concurrently through the circuit if the total delay time through a circuit is larger than the pulse width [5]. This allows the synchronous memory to adopt the pipelining to obtain a fast column data path [4].

3. Simulation Results

The speed and leakage current of the proposed self-timed dual V_T logic have been assessed via SPICE simulations. The V_T's of high V_T and low V_T N-MOS and P-MOS used in simulations are 0.65 V, 0.20 V, −0.70 V and −0.22 V, respectively. The subthreshold swings S are assumed to be 110 mV/dec for N-MOS transistors and 120 mV/dec for P-MOS transistors at 85°C. The load has a capacitance value equivalent to 3389 μm MOS width. For the comparison, simulation was carried out with a single low-V_T CMOS logic and a conventional dual V_T logic with γ=0.26 under the same conditions. The inverter fan-out is fixed to be 3 in the single V_T and the dual V_T logic circuits. In the proposed self-timed logic, the fan-outs of high-V_T NMOS and high-V_T PMOS transistors are chosen to be 6 and 3, respectively, for the equal rising and falling times of the pulses. The total area of the circuits in simulations are chosen to be nearly the same.

Figure 2 shows the simulated wave forms of a pulse propagation through a 5-inverter chain at 1.5 V.

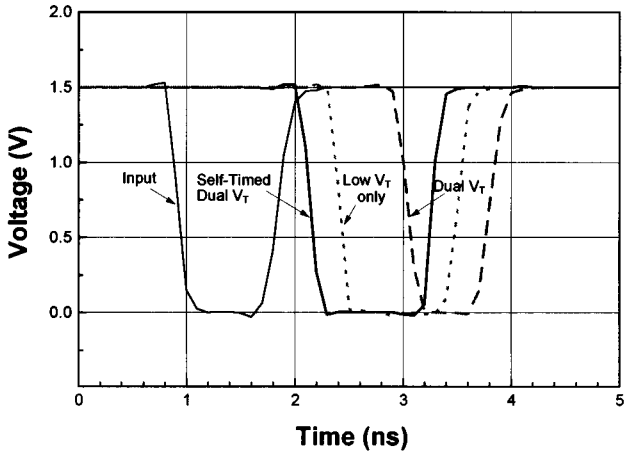

Fig. 2 Simulated voltage waveforms for the proposed self-timed logic of Fig. 1, the conventional dual V_T logic and a single low V_T logic. The conventional dual V_T and the single low V_T logic have the same number of inverter stages and load capacitor as the circuit of Fig. 1.

The active low input signal is transformed into a pulse of 0.8 ns width. The output follows the input pulse after a 1.3 ns delay in the proposed logic, while the single low V_T logic outputs a pulse after a 1.4 ns delay. The fast operation of the proposed circuit results from the reduced gate capacitance. The propagation delay of the active transition in the conventional dual V_T logic amounts to 2.2 ns. The conventional dual V_T logic cannot reproduce the input pulse shape because the pulse width is too narrow for the circuit to follow. The leakage current of the proposed self-timed logic is 20.2 pA which is the same as that of the dual V_T logic, compared to 27.5 nA of the single V_T logic.

4. Conclusions

A new dual V_T self-timed logic is proposed to reduce the subthreshold current, a critical problem in low voltage CMOS logic, by nearly 1360 times. The proposed circuit removes the limitation in γ of the dual V_T logic to ensure 6 times higher speed operation. Its pulse operation achieves concurrent propagation of multiple signals through the circuit. This pipelining nature can be used to enhance the speed of the multi-giga bit synchronous DRAM's [4].

Acknowledgments

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